CLAIMS

1. A method of fabricating a flash memory device including an array of split gate cells, comprising the steps of:

providing a silicon substrate having a top surface;

implanting ions into a predefined area of said substrate to form a common source region of said substrate;

forming at least one floating gate over said substrate, each said floating gate being associated with one of the cells and having a portion which overlies a portion of said common source region, the overlying portion of each floating gate providing for a high coupling ratio for the associated flash cell;

forming a select gate over at least a portion of each said floating gate; and

forming a drain region associated with each said cell.

2. A method of fabricating a flash memory device as recited in claim 1, wherein said step of implanting a common source region on said substrate includes the steps of:

patterning a photoresist disposed over said substrate to substantially define said predefined area at which the common source region is to be formed;

implanting said ions into said substrate to form said common source region of said substrate using said patterned photoresist as an implant mask; and

removing said patterned photoresist.

3. A method of fabricating a flash memory device as recited in claim 2, wherein said ions include arsenic ions.

4. A method of fabricating a flash memory device as recited in claim 1, wherein said step of implanting ions into a region of said substrate includes the steps of:

forming a sacrificial oxide layer over said top surface of said substrate;

patterning a photoresist disposed over said substrate to substantially define said predefined area at which the common source region is to be formed;

implanting said ions into said substrate to form said common source region of said substrate using said patterned photoresist as an implant mask; and

removing said patterned photoresist and said sacrificial oxide layer.

5. A method of fabricating a flash memory device as recited in claim 1, wherein said step of forming at least one floating gate over said substrate includes the steps of:

forming a tunneling oxide layer over the exposed top surface of said substrate;

depositing a first polysilicon layer over said tunneling oxide layer;

depositing a nitride masking layer over said first polysilicon layer;

patterning and etching said nitride masking layer to expose at least one first portion and at least one second portion of said first polysilicon layer, said first and second exposed portions substantially defining first and second floating gate regions;

forming a floating gate oxide layer over said first and second exposed portions of said first polysilicon layer;

removing said nitride masking layer;

etching said first polysilicon layer and said tunneling oxide layer using said floating gate oxide layer as a mask leaving remaining portions of said first polysilicon layer and said tunneling oxide layer disposed beneath said floating gate oxide layer, and exposing a portion of said substrate, each said remaining portion of said first polysilicon layer forming one of said floating gates associated with said cell and having side walls and also having a portion which overlies a portion of said common source region there by providing a high coupling ratio for an associated cell.

6. A method of fabricating a flash memory device as recited in claim 5, wherein said step of forming at least one select gate over at least a portion of said floating gate includes the steps of:

forming an insulating layer over said exposed portion of said substrate, over said floating gate oxide layer, and over said floating gates;

forming a second polysilicon layer over said insulating layer;

forming a conductive layer over said second polysilicon layer; and

removing portions of said conductive layer, said second polysilicon layer, and said insulating layer to form a plurality of select gates each having a portion overlying a portion of an associated one of said floating gates.

7. A method of fabricating a flash memory device as recited in claim 6, wherein said step of forming an insulating layer over said exposed portion of said substrate, over said floating gate oxide layer, and over said floating gates includes the steps of:

forming a first gate oxide layer over said exposed portion of said substrate, over said floating gate oxide layer, and over said floating gates;

forming a nitride layer over said first oxide layer;

performing an etching process to remove a portion of said nitride layer and leaving nitride spacers adjacent said side walls of each of said floating gates; and

forming a second gate oxide layer over said first oxide layer, over said nitride spacers and over said floating gate oxide layer.

8. A method of fabricating a flash memory device as recited in claim 6, wherein said conductive layer includes tungsten.

9. A method of fabricating a flash memory device as recited in claim 1, wherein said ions includes Boron ions.

10. A method of fabricating a flash memory device as recited in claim 6, wherein said step of forming a drain region associated with each cell includes the step of:

patterning and etching said conductive layer and portions of said substrate to substantially define the boundaries of at least one drain area of said substrate; and

implanting ions into said drain area of said substrate to form at least one drain region.

11. A method of fabricating a flash memory device as recited in claim 4, wherein said step of implanting said ions into said substrate to form said common source region of said substrate using said patterned photoresist as an implant mask includes:

implanting arsenic ions to provide a dopant density in the range of 1 x 10^{14}/cm2 to 5 x $10^{14}/cm^2$ and at an energy range of 80 to 150 KeV.

12. A method of fabricating a flash memory device as recited in claim 5, wherein said step of depositing a first polysilicon layer over said tunneling oxide layer includes:

depositing said first polysilicon layer at a temperature of approximately 620 degrees C in order to form said first polysilicon layer having a thickness in the range of 500 to 2500 angstroms.

13. A method of fabricating a flash memory device as recited in claim 12, wherein said first polysilicon layer includes SiH4.

14. A method of fabricating a flash memory device having a high coupling ratio, comprising the steps of:

providing a silicon substrate having a top surface;

forming a sacrificial oxide layer over said top surface of said substrate;

patterning a photoresist layer disposed over said sacrificial oxide layer to substantially define a source region of the substrate;

implanting first ions into said substrate to form a common source region of said substrate using the patterned photoresist layer as an implant mask;

removing said patterned photoresist layer and said sacrificial oxide layer to expose said top surface of said substrate;

forming a tunneling oxide layer over the exposed top surface of said substrate;

depositing a first polysilicon layer over said tunneling oxide layer;

depositing a nitride masking layer over said first polysilicon layer;

patterning and etching said nitride masking layer to expose at least one first portion and at least one second portion of said first polysilicon layer, said first and second exposed portions substantially defining first and second floating gate regions;

forming a floating gate oxide layer over said first and second exposed portions of said first polysilicon layer;

removing said nitride masking layer;

etching said first polysilicon layer and said tunneling oxide layer using said floating gate oxide layer as a mask leaving remaining portions of said first polysilicon layer and said tunneling oxide layer disposed beneath said floating gate oxide layer, and exposing a portion of said substrate, each said remaining portion of said first polysilicon layer forming a floating gate

associated with a cell and having side walls and also having a portion which overlies a portion of said common source region there by providing a high coupling ratio for an associated cell;

forming a first gate oxide layer over said exposed portion of said substrate, over said floating gate oxide layer, and over said floating gates;

forming a nitride layer over said first oxide layer;

performing an etching process to remove a portion of said nitride layer and leaving nitride spacers adjacent said side walls of each of said floating gates;

forming a second gate oxide layer over said first oxide layer, over said nitride spacers and over said floating gate oxide layer

forming a second polysilicon layer over said second gate oxide layer;

forming a conductive layer over said second polysilicon layer;

removing portions of said conductive layer, said second polysilicon layer, said second gate oxide layer, said nitride spacers and said first gate oxide layer to form a plurality of select gates each having a portion overlying a portion of an associated one of said floating gates; and

patterning and etching said conductive layer to expose portions of said substrate to substantially define the boundaries of at least one drain area of said substrate; and

implanting second ions into said drain area of said substrate to form at least one drain region.

15. A method of fabricating a flash memory device having a high coupling ratio as recited in claim 14, further including the step of:

implanting additional ions into portions of said substrate defined by said first and second floating gate regions, in order to adjust the threshold voltage of the flash memory cells.

16. A method of fabricating a flash memory device as recited in claim 15, wherein said first ions include N-type ions and said additional ions include P-type ions, whereby threshold voltages of the flash memory cells are adjusted.

17. A flash memory device having a high coupling ration formed in accordance with a process, comprising the steps of:

providing a silicon substrate having a top surface;

implanting ions into a predefined area of said substrate to form a common source region of said substrate;

forming at least one floating gate over said substrate, each said floating gate being associated with one of the cells and having a portion which overlies a portion of said common source region, the overlying portion of each floating gate providing for a high coupling ratio for the associated flash cell;

forming a select gate over at least a portion of each said floating gate; and

forming a drain region associated with each said cell..

18. A flash memory device having a high coupling ration as recited in claim 17, formed in accordance with a process, including the step of:

implanting additional ions into portions of said substrate defined by said first and second floating gate regions, in order to adjust the threshold voltage of the flash memory cells.

19. A flash memory device having a high coupling ration as recited in claim 17, formed in accordance with a process, including the steps of:

patterning a photoresist disposed over said substrate to substantially define said predefined area at which the common source region is to be formed;

implanting said ions into said substrate to form said common source region of said substrate using said patterned photoresist as an implant mask; and

removing said patterned photoresist.

20. A flash memory device having a high coupling ration as recited in claim 17, formed in accordance with a process, including the steps of:

forming a tunneling oxide layer over the exposed top surface of said substrate;

depositing a first polysilicon layer over said tunneling oxide layer;

depositing a nitride masking layer over said first polysilicon layer;

patterning and etching said nitride masking layer to expose at least one first portion and at least one second portion of said first polysilicon layer, said first and second exposed portions substantially defining first and second floating gate regions;

forming a floating gate oxide layer over said first and second exposed portions of said first polysilicon layer;

removing said nitride masking layer;

etching said first polysilicon layer and said tunneling oxide layer using said floating gate oxide layer as a mask leaving remaining portions of said first polysilicon layer and said tunneling oxide layer disposed beneath said floating gate oxide layer, and exposing a portion of said substrate, each said remaining portion of said first polysilicon layer forming one of said floating gates associated with said cell and having side walls and also having a portion which overlies a portion of said common source region there by providing a high coupling ratio for an associated cell.